

**AMENDMENTS TO THE CLAIMS:**

This listing of claims will replace all prior versions, and listings, of claims in the application.

**LISTING OF CLAIMS:**

Claims 1-18 (Canceled).

19. (New) An electronic system, comprising:  
at least one input/output device; and  
an integrated circuit, coupled to the at least one input/output device, and comprising  
functional circuitry for executing logical operations upon digital data signals  
in a synchronous fashion; and  
access circuitry coupled to said functional circuitry and further coupled to a  
memory core in said integrated circuit for asynchronously accessing said memory core more  
than once in a single clock cycle.

20. (New) The electronic system of Claim 19, wherein said electronic system is  
a cellular telephone.

21. (New) The electronic system of Claim 19, wherein said memory core is part  
of a dual-access RAM.

22. (New) The electronic system of Claim 19, wherein said memory core and  
said access circuitry combine to form a multiple access memory core.

23. (New) The electronic system of Claim 19, wherein said access circuitry is  
embodied in an electronic device coupling a memory interface unit to said memory core.

24. (New) The electronic system of Claim 19, wherein said electronic system is  
a digital signal processor.

25. (New) The electronic system of Claim 19, wherein said memory core is part  
of a core of a processor.

26. (New) The electronic system of Claim 19, wherein addresses accessed in  
said memory core are adjacent addresses.

27. (New) The electronic system of Claim 19, wherein address accessed in said  
memory core are non-adjacent addresses.

28. (New) An electronic system, comprising:  
at least one input/output device; and  
an integrated circuit, coupled to the at least one input/output device, and comprising:  
functional circuitry for executing logical operations upon digital data signals  
in a synchronous fashion; and  
access circuitry coupled to a memory core in said integrated circuit for accessing  
said memory core more than once in a single clock cycle wherein self-timing logic provides  
signals that facilitate said accessing.

29. (New) The electronic system of Claim 28, wherein said electronic system is  
a cellular telephone.

30. (New) The electronic system of Claim 28, wherein said memory core is part  
of a dual-access RAM.

31. (New) The electronic system of Claim 28, wherein said memory core and  
said circuitry combine to form a multiple access memory core.

32. (New) The electronic system of Claim 28, wherein said access circuitry is  
embodied in an electronic device coupling a memory interface unit to said memory core.

33. (New) The electronic system of Claim 28, wherein said electronic system is  
a digital signal processor.

34. (New) The electronic system of Claim 28, wherein said memory core is part  
of a core of a processor.

35. (New) The electronic system of Claim 28, wherein addresses accessed in  
said memory core are adjacent addresses.

36. (New) The electronic system of Claim 28, wherein address accessed in said  
memory core are non-adjacent addresses.

37. (New) A memory module, comprising:  
a memory interface unit;  
a memory core; and  
circuitry for coupling said memory interface unit to said memory core and enabling  
access to said memory core at least two times in a single clock cycle.

38. (New) The memory module of Claim 37, wherein said circuitry for coupling  
said memory interface unit to said memory core comprises:  
a multiplexer having a first input coupled to a first address bus and a second input  
coupled to receive a second address bus and an output coupled to an input of said memory  
core; and

logic circuitry having an input coupled to receive an output signal from said memory core and an output coupled to an input of said multiplexer.

39. (New) The memory module of Claim 38, wherein said output signal from said memory core is a signal that indicates that the hold time on the address bus is achieved.

40. (New) The memory module of Claim 38, wherein said output signal from said memory core is a signal that indicates that the hold time on the address bus is achieved and that it is possible to present a new address on the bus.

41. (New) The memory module of Claim 38, wherein said logic circuitry is self-timing.

42. (New) The memory module of Claim 41, wherein said self-timing logic circuitry is used for addressing and for switching data that must be written in said memory core.

43. (New) The memory module of Claim 41, wherein said self-timing logic circuitry facilitates a dissociation between what is clocked on the system clock and access to the memory core.

44. (New) The memory module of Claim 37, wherein said memory core is a single-access memory core.

45. (New) The memory module of Claim 37, wherein said circuitry for coupling said memory interface unit to said single-access memory core comprises:

a multiplexer having a first input coupled to a first address bus and a second input coupled to receive a second address bus and an output coupled to an input of said memory core; and

delay circuitry having an input coupled to receive a signal for input to said memory core and an output coupled to an input of said multiplexer.

46. (New) The memory module of Claim 45, wherein said signal for input to said memory core is a strobe signal.

47. (New) The memory module of Claim 37, wherein an address bus, a data in bus, a data out bus, a first signal line for an access ready signal, a second signal line for an output ready signal, and at least two signal lines for strobe signals couple said circuitry to said memory core.

48. (New) The memory module of Claim 37, wherein said memory module is accessed by a first bus and a second bus while addresses of a third bus and a fourth bus are temporarily dispatched to said memory core.

49. (New) The memory module of Claim 37, wherein a first bus address is switched using a signal from a system clock while a second address bus is switched using a signal other than from said system clock.

50. (New) The memory module of Claim 37, wherein addresses accessed in said memory core are adjacent addresses.

51. (New) The memory module system of Claim 37, wherein address accessed in said memory core are non-adjacent addresses.

52. (New) A processing apparatus, comprising:  
a processing engine; and  
a processor backplane coupled to said processing engine, said processor backplane comprising a memory module, said memory module, comprising:  
a memory interface unit;  
a memory core; and  
circuitry for coupling said memory interface unit to said memory core and enabling access to said memory core at least two times in a single clock cycle.

53. (New) The processor backplane of Claim 52, wherein a bus couples said memory module to said processing engine.

54. (New) The processing apparatus of Claim 52, wherein said processor backplane further comprises a memory cache coupled to said processing engine.

55. (New) The processing apparatus of Claim 52, wherein said processor backplane further comprises at least one peripheral device coupled to said processing engine.

56. (New) The processing apparatus of Claim 52, wherein said processor backplane further comprises an external interface coupled to said processing engine.

57. (New) The processing apparatus of Claim 52, wherein said processing engine comprises a processing core coupled to a memory management unit.

58. (New) The processing apparatus of Claim 57, wherein said processing core is a central processing unit.

59. (New) The processing apparatus of Claim 57, wherein said processing core comprises:  
an instruction buffer unit;  
a program flow unit;  
an address data flow unit; and  
a data computation unit coupled to said instruction buffer unit, said program flow unit and said address flow unit.

60. (New) The processing apparatus system of Claim 52, wherein addresses accessed in said memory core are adjacent addresses.

61. (New) The processing apparatus of Claim 52, wherein address accessed in said memory core are non-adjacent addresses.